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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/682,166	10/10/2003	Koichi Ishimi	67161-116	8198

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EXAMINER	
NGUYEN, LINH M	
ART UNIT	**PAPER NUMBER**
2816	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/18/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

IV

Office Action Summary	**Application No.** 10/682,166	**Applicant(s)** ISHIMI, KOICHI
	Examiner Linh M. Nguyen	**Art Unit** 2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,4,6-9,11-17,19-26,55-62 and 75-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6,8,9,11,12,15-17,19-26,55-62 and 75-79* is/are allowed.

6)☒ Claim(s) *3,4,7,13 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413)
Paper No(s)/Mail Date. *12/12/06*.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action replaces the office action mailed on 07/14/2006. The purpose for this office action is to withdraw the finality (through inadvertent error); as such, the status of this action is non-final.

This is a reply to the Applicant's RCE filing and amendment submitted on 06/15/2006. By virtue of this amendment, claims 3-4, 6-9, 11-17, 19-26, 55-62 and 75-79 are now pending.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 3, 4, 7, 13 and 14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The newly added limitations *"the difference between the logic low and the logic high period of said output clock signal is maintained"* and *"maintaining that duty ratio of said output clock signal* are not described in the specification of the instant application. Such a missing description of the limitations would make the claimed invention unclear and causes difficulty in making distinction with prior art.

Allowable Subject Matter

3. Claims 3-4, 6-9, 11-17, 19-26, 55-62 and 75-79 are allowed.

4. The following is a statement of reasons for the indication of allowable subject matter:

5. The Applicant is noted that claims 3,4,7,13 and 14 must be corrected to overcome 112 1st paragraph rejection set forth in this office action in order for these claims to be allowed.

The closest prior art of record does not show or fairly suggest:

a) A clock generation circuit, in which the difference between the logic low period and the logic high period of the output clock signal is maintained, as called for in claims 3, 4, 7, 13 and 14;

b) A clock generation circuit including a control circuit incrementing/decrementing a digital count value in response to a rising/falling of a reference clock signal, and a ring oscillator including a delay line varying a delay time in accordance with the digital count value, in combination with the remaining claimed limitations, as called for in claims 6, 19 and 79;

c) A clock generation circuit, in which in a duty ratio control signal, a period of time during which both of clock signal and the duty ratio control signal are logic high is different from the other period of time, in combination with the remaining claimed limitations, as called for in claim 8;

d) A clock generation circuit, in which in a duty ratio control signal, a period of time during which both of clock signal and the duty ratio control signal are logic low is different from the other period of time, in combination with the remaining claimed limitations, as called for in claim 9;

e) A clock generation circuit, in which a plurality of first transistors connected in parallel between a power supply node and an output node and having one polarity and a driving capability control portion controlling on/off of the plurality of first and second transistors respectively using a plurality of driving capability control signals, in combination with the remaining claimed limitations, as called for in claim 11;

f) A clock generation circuit, in which a timing control portion controlling rising or falling timing of a signal level output from a first inverter circuit to a second inverter circuit using a plurality of timing control signals, in combination with the remaining claimed limitations, as called for in claim 12;

g) A clock generation circuit, in which a delay circuit capable of controlling a delay time using a delay control signal and a logic element receiving an output signal from the delay circuit and the reference clock signal for outputting a clock signal, in combination with the remaining claimed limitations, as called for in claim 15;

h) A clock generation circuit, in which a logic element receiving a selector control signal and a clock signal for outputting a select signal, in combination with the remaining claimed limitations, as called for in claim 22;

i) A clock generation circuit, in which in a duty ratio control signal, a period of time during which both of clock signal and the duty ratio control signal are logic high and the other period of time varies, in combination with the remaining claimed limitations, as called for in claim 25;

j) A clock generation circuit, in which in a duty ratio control signal, a period of time during which both of clock signal and the duty ratio control signal are logic low and the other period of time varies, in combination with the remaining claimed limitations, as called for in claim 26;

k) A system including a current measurement circuit measuring an operating current of a circuit receiving clock signal, in which a central processing unit controls a duty ratio of the clock signal or on/off of duty ratio control based on a measurement result of the operating current, in combination with the remaining claimed limitations, as called for in claims 55 and 56;

l) A system including a temperature measurement circuit measuring a temperature of a circuit receiving clock signal, in which a central processing unit controls a duty ratio of the clock signal or on/off of duty ratio control based on a measurement result of the temperature, in combination with the remaining claimed limitations, as called for in claims 59 and 60; and

m) A system, in which a duty ratio of a clock signal can be set by an instruction from a central processing unit, individually for the clock signal being supplied to a module circuit and for the clock signal being supplied to a prescribed external circuit, in combination with the remaining claimed limitations, as called for in claims 75 and 76.

Remarks

5. Applicant's argument filed 06/15/2006 has been seriously considered but not completely persuasive.

Regarding Applicant's arguments with respect to claims 3, 4, 13 and 14, on pages 21-22, last paragraph bridging page 22, the Applicant states that *Yen does not disclose at least one buffer circuit buffering said output clock signal such that a logic low period and a logic high period of said output clock signal are different from each other, and the difference between the logic low period and the logic high period of the output clock signal is maintained," recited in* *claims 3 and 4; or at least one buffer circuit for changing a duty ratio of said output clock signal and maintaining that duty ratio of said output clock signal, recited in claims 13 and 14.* The examiner partially disagrees. Yen clearly discloses, in Fig. 7B, that a logic low period and a logic high period of said output clock signal are different from each other by comparing FCLK and MCLK, this also denotes changing a duty ratio of said output clock signal. Regarding the limitations of *the difference between the logic low period and the logic high period of the output clock signal is maintained* and *maintaining that duty ratio of said output clock signal,* as set forth in the office action the limitations lack support in the specification, and since Yen does not disclose these limitations claims 3, 4, 7, 13 and 14 are allowable; however, if these newly added limitations are to be deleted, the rejection set forth in the office action dated 02/15/2006 still applies.

With respect to claim 7, on page 24, last paragraph, similar argument has been addressed, it is suggested to refer to the response stated in the above paragraph.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER